

CLAIMS

What is claimed is:

1 1. A method comprising:
2 selecting one or more of three access methods
3 provided in an integrated circuit to debug program
4 code and/or circuitry contained therein, the three
5 access methods including,
6 a serial debug access through a serial I/O test
7 port of the integrated circuit,
8 a parallel I/O mapped debug access through a
9 host I/O port of the integrated circuit, and
10 a parallel direct debug access through I/O pads
11 of the integrated circuit.

1 2. The method of claim 1, wherein
2 the selecting of the one or more three access methods
3 includes
4 setting a test mode input on an I/O pad of the
5 integrated circuit.

1 3. The method of claim 1, wherein
2 the parallel direct debug access is through host I/O
3 pads around circuitry of the host I/O port.

1 4. The method of claim 1, further comprising:
2 debugging the integrated circuit using test/debug
3 instructions and data.

1 5. The method of claim 4, wherein
2 the debugging of the integrated circuit includes
3 setting a plurality of registers in the integrated
4 circuit to control the debugging of the integrated
5 circuit.

1 6. The method of claim 5, wherein
2 the plurality of registers in the integrated circuit
3 control a debug controller in the integrated circuit to
4 control the debugging.

1 7. The method of claim 5, wherein
2 the serial debug access method is selected and the
3 setting of the plurality of registers is serially
4 performed.

1 8. The method of claim 5, wherein
2 the parallel I/O mapped debug access method is
3 selected and the setting of the plurality of registers is
4 performed in parallel by memory map addressing of the
5 plurality of registers and the data therein.

1 9. The method of claim 5, wherein
2 the parallel direct debug access method is selected
3 and the setting of the plurality of registers is performed
4 in parallel directly addressing each of the plurality of
5 registers and the data therein.

1 10. The method of claim 2, wherein
2 the setting of the test mode input controls a select
3 input control of a multiplexer in the integrated circuit
4 to select between parallel I/O mapped debug access and
5 parallel direct debug access to debug the integrated
6 circuit.

1 11. An integrated circuit comprising:
2 debug registers to control on-chip testing and
3 debugging of the integrated circuit;
4 a serial test port to access the debug registers
5 serially;

6 a host I/O port to access the debug registers in
7 parallel using I/O memory mapped access; and
8 I/O pads to access the debug registers in
9 parallel using direct access.

1 12. The integrated circuit of claim 11, further
2 comprising:
3 a multiplexer to select between loading the debug
4 registers in parallel with the host I/O port and the I/O
5 pads.

1 13. The integrated circuit of claim 12, wherein
2 the multiplexer is responsive to a test mode input of
3 an I/O pad.

1 14. The integrated circuit of claim 11, further
2 comprising:
3 a demultiplexer to select between reading information
4 from the debug registers in parallel with the host I/O
5 port and the I/O pads.

1 15. The integrated circuit of claim 14, wherein
2 the demultiplexer is responsive to a test mode input
3 of an I/O pad.

1 16. The integrated circuit of claim 11, further
2 comprising:
3 one or more digital signal processing units to test
4 and debug.

1 17. The integrated circuit of claim 11, further
2 comprising:
3 one or more functional blocks having circuitry to
4 test and debug.

1 18. The integrated circuit of claim 11, further
2 comprising:
3 one or more memories having program code to test and
4 debug.

1 19. The integrated circuit of claim 11, further
2 comprising:
3 a global memory having program code to test and
4 debug.

1 20. The integrated circuit of claim 11, further
2 comprising:
3 a debug controller coupled to the debug registers,
4 the debug controller to test and debug circuitry within
5 the integrated circuit in response to the information
6 stored in the debug registers.

1 21. The integrated circuit of claim 20, wherein
2 the information stored in the debug registers is one
3 or more debug instructions of the set of break execution,
4 inject command, single step, reset, break at address, and
5 PRAM.

1 22. A integrated circuit test system comprising:
2 an integrated circuit including,
3 debug registers to control on-chip testing and
4 debugging of the integrated circuit,
5 a serial test port to load the debug registers
6 serially,
7 a host I/O port to load the debug registers in
8 parallel using I/O memory mapped access, and
9 I/O pads to load the debug registers in
10 parallel using direct access;
11 and

12 a tester including,
13 a processor readable storage medium, and
14 code recorded in the processor readable
15 storage medium
16 to test and debug the integrated circuit,
17 to interface the tester to the serial test
18 port of the integrated circuit to load the debug
19 registers serially,
20 to interface the tester to the host I/O
21 port of the integrated circuit to load the debug
22 registers in parallel using I/O memory mapped
23 access, and
24 to interface the tester to the I/O pads of
25 the integrated circuit to load the debug
26 registers in parallel using direct access.

1 23. The integrated circuit test system of claim 22,
2 wherein
3 the processor readable storage medium is one or more
4 of the set of magnetic storage medium, optical storage
5 medium, or semiconductor storage medium.

1 24. The integrated circuit test system of claim 22,
2 wherein the integrated circuit further includes
3 a multiplexer to select between loading the
4 debug registers in parallel with the host I/O port
5 and the I/O pads.

1 25. The integrated circuit test system of claim 24,
2 wherein
3 the multiplexer is responsive to a test mode input of
4 an I/O pad.

1 26. The integrated circuit test system of claim 22,
2 wherein
3 the integrated circuit is a packaged integrated
4 circuit and the tester is a packaged integrated circuit
5 tester to test and debug the packaged integrated circuit.

1 27. The integrated circuit test system of claim 22,
2 wherein
3 the integrated circuit is packaged and coupled to a
4 printed circuit board and the tester is a printed circuit
5 board tester to test and debug the printed circuit board
6 including the integrated circuit.

1 28. The integrated circuit test system of claim 22,
2 wherein
3 the integrated circuit is packaged and coupled to a
4 printed circuit board which is inserted into a system and
5 the tester is a system tester to test and debug the system
6 and the printed circuit board including the integrated
7 circuit.